EXHIBIT C

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--==========================================================--
--                                                          --
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--   DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING      --
--   RAPID PROTOTYPING LABORATORY                           --
--                                                          --
--   FILE          | add_sub.vhd                            --
--   -------------+----------------------------------       --
--   DESCRIPTION   | Module to perform addition or          --
--                 | subtraction.                           --
--   -------------+----------------------------------       --
--   AUTHOR        | Pavle Belanovic                        --
--   -------------+----------------------------------       --
--   DATE          | 20 June 2002                           --
--                                                          --
--==========================================================--

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--                                                                             --
--*****************************************************************************--

--==========================================================--
--                       LIBRARIES                          --
--==========================================================--

-- IEEE Libraries --
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

-- float
library work;
use work.float_pkg.all;

----------------------------------------------------------------
--                    Add/Sub Module                          --
----------------------------------------------------------------
entity add_sub is
    generic
    (
        man_bits              :   integer :=
    );
    port
    (
--===========================================================--
--                                                           --
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--  RAPID PROTOTYPING LABORATORY                             --
--                                                           --
--  FILE          | parameterzied_priority_encoder.vhd       --
--  --------------+------------------------------------     --
--  DESCRIPTION   | Parameterized priority encoder           --
--  --------------+------------------------------------     --
--  AUTHOR        | Pavle Belanovic                          --
--  --------------+------------------------------------     --
--  DATE          | 20 June 2002                             --
--                                                           --
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--                                                                         --
--*************************************************************************--

--===========================================================--
--                        LIBRARIES                          --
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-- IEEE Libraries --
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

-- float
library work;
use work.float_pkg.all;

-------------------------------------------------------------
--          Parameterized priority encoder                 --
-------------------------------------------------------------
entity parameterized_priority_encoder is
    generic
    (
        man_bits        :   integer := 0;
        shift_bits   :   integer := 3
    );
    port
    (
--connect output signals
OUT1(exp_bits+man_bits_out)                                              <=
s_out;
OUT1(exp_bits+man_bits_out-1 downto man_bits_out)    <=   e_out;
OUT1(man_bits_out-1 downto 0)                                            <=
f_out;

--instatiate components
--normalizer
norm: normalizer
    generic map
    (
        exp_bits            =>  exp_bits,
        man_bits            =>  man_bits_in
    )
    port map
    (
        --inputs
        MAN_IN              =>  f_in,
        EXP_IN              =>  e_in,
        READY                   =>  READY,
        CLK                     =>  CLK,
        EXCEPTION_IN    =>  EXCEPTION_IN,
        --outputs
        MAN_OUT             =>  f_int,
        EXP_OUT             =>  e_int,
        EXCEPTION_OUT   =>  exc_int,
        DONE                    =>  rd_int
    );
--round_add
rnd_add: round_add
    generic map
    (
        man_bits_in     =>  man_bits_in,
        man_bits_out    =>  man_bits_out
    )
    port map
    (
        --inputs
        MAN_IN              =>  f_int,
        READY                   =>  rd_int,
        CLK                     =>  CLK,
        ENABLE              =>  round_int,
        EXCEPTION_IN    =>  exc_int,
        --outputs
        MAN_OUT             =>  f_out,
        EXCEPTION_OUT   =>  EXCEPTION_OUT,
        DONE                    =>  DONE
    );
--SYNCHRONOUS
main: process (CLK)
begin
    if(rising_edge(CLK)) then
        --pipelining sign bit
        s_out           <=  s_int;
        s_int           <=  s_in;
        --pipelining exponent
        e_out           <=  e_int;
        --pipelining rounding
        round_int   <=  ROUND;
    end if;--CLK
    end process;--main
end rnd_norm_arch;--end of architecture

```